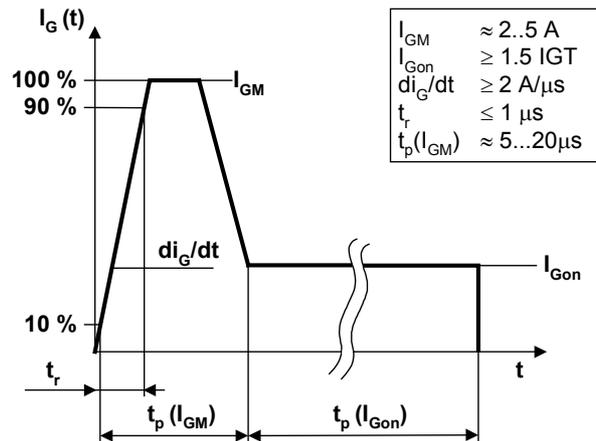


Gate-drive Recommendations for Phase Control Thyristors



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Product Information

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1 Introduction

The main purpose of a Gate-driver for a phase control thyristor (PCT) is to provide a gate current of the right amplitude, at the right time, and of the right duration. This would seem simple, but the analysis of failed thyristors due to inadequate gate pulses leads to the conclusion that the proper design of a Gate-drive unit is not trivial. This application note points out some of the most important Gate-drive design rules.

A thyristor is a current-controlled bipolar semiconductor, unlike MOSFETs or IGBTs which are voltage controlled. Therefore, a thyristor Gate-drive unit is primarily a current source, supplying a specifically shaped current pulse from gate to the cathode. The voltage drop along the gate-to-cathode path is a function of the gate current, the anode current and the internal impedance between gate and cathode. For this reason, thyristor manufacturers specify gate current pulses rather than gate voltage pulses.

2 Gate-drive recommendations and application aspects

2.1 Definitions

To explain the definitions of triggering data for ABB thyristors we use as an example the triggering data table from the data sheet for 5STB 18U6500.

Triggering

Maximum rated values ¹⁾

Parameter	Symbol	Conditions	min	typ	max	Unit
Peak forward gate voltage	V_{FGM}				12	V
Peak forward gate current	I_{FGM}				10	A
Peak reverse gate voltage	V_{RGM}				10	V
Gate power loss	P_G	For DC gate current			3	W
Average gate power loss	P_{GAV}		see Fig. 1			

Characteristic values

Parameter	Symbol	Conditions	min	typ	max	Unit
Gate trigger voltage	V_{GT}	$T_j = 25^\circ\text{C}$			2.6	V
Gate trigger current	I_{GT}	$T_j = 25^\circ\text{C}$			400	mA
Gate non-trigger voltage	V_{GD}	$V_D = 0.4 \times V_{DRM}, T_{vjmax} = 110^\circ\text{C}$	0.3			V
Gate non-trigger current	I_{GD}	$V_D = 0.4 \times V_{DRM}, T_{vjmax} = 110^\circ\text{C}$	10			mA

¹⁾ Maximum Ratings are those values beyond which damage to the device may occur.

Table 1 Tabular trigger data for device 5STB 18U6500.

V_{FGM} : Peak forward gate voltage. This voltage may instantaneously occur across the gate and cathode terminals if a strong initial gate pulse with a short rise time and high amplitude is applied and the anode current rises with a high di/dt.

I_{FGM} : This value indicates the maximum allowable gate current primarily limited by the gate contact. It is a maximum rating, valid for short pulses $\leq 100 \mu\text{s}$. For DC operation, I_{FGM} must be reduced further in order not to exceed the maximum continuous gate power losses P_G . Applying an I_{FGM} above the limiting value may be destructive due to over stress of the internal gate contact interfaces even if the average gate power is within the given limits.

V_{RGM} : Peak reverse gate voltage. Exceeding this rating will cause excessive reverse gate power losses.

P_G : Gate power loss. This is the maximum continuous gate power the thyristor can withstand without being damaged in the gate region.

V_{GT} , I_{GT} : Gate trigger voltage and current, respectively, defined as the minimum gate voltage/current necessary to trigger the thyristor. These parameters are measured with an anode voltage of 6 V at 25 °C. V_{GT} and I_{GT} decrease with increasing anode voltage and temperature. Note that these values are measured at quasi-stationary conditions. As explained later is a proper margin to these values needed for triggering at dynamic conditions.

V_{GD} , I_{GD} : Gate non-trigger voltage and current, respectively, defined as the maximum admissible gate voltage/current to avoid spurious triggering of the thyristor. These ratings are defined at quasi worst-case conditions of $V_D = 0.4 \cdot V_{DRM}$ and T_{vjmax} . and will have higher values at reduced anode voltage and junction temperature. V_{GD} and I_{GD} are of particular importance in a noisy environment where electromagnetic interference can lead to undesired thyristor triggering. This may not only cause a malfunction of the converter, but is also dangerous for the thyristor because local firing may destroy the amplifying gate structure. Special measures like gate signal filtering have to be implemented in this case.

In addition to the table data, the data sheet also includes a gate characteristic curve, see figure 1.

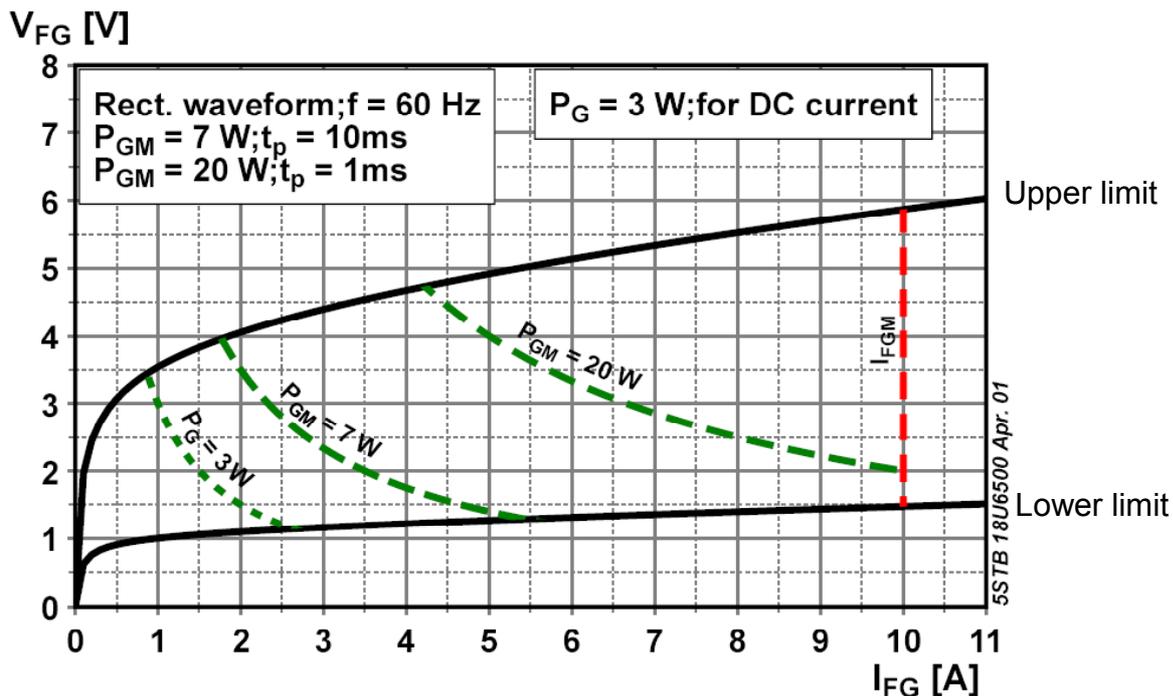


Figure 1 Gate characteristics curve from the data sheet for 5STB 18U6500.

This curve shows the spread of V_{FG} as a function of I_{FG} considering both effects of temperature, within the whole operational temperature range, and whether the voltage is measured under static or dynamic conditions. The lower limit is the minimum expected DC gate voltage at $T_j = -40$ °C and the upper limit the highest expected dynamic gate voltage at T_{vjmax} . The dotted hyperbolic lines show the instantaneous gate power limits for DC-current and for two different pulse conditions while the vertical dotted line gives the absolute gate current limit of 10 A.

2.2 Gate design and characteristics for ABB thyristors

Small area devices can be triggered properly by a relatively moderate current applied to a small gate region in the center of the device. For large area devices of similar gate design a substantial current would be required and it would also then take a relatively long time to get the whole device conducting. To avoid these problems an amplifying gate with interdigitation is used in large area devices from ABB. The amplifying gate allows even the largest thyristors to be triggered with a low external gate current. This is achieved by integrated gate current amplification and allows the user to trigger all ABB PCT's with the same gate unit design. The amplifying gate consists of an auxiliary thyristor integrated in the main thyristor. This auxiliary thyristor is first triggered and supplies the needed gate trigger current for the main thyristor. Schematics showing the working principle and its implementation into the silicon wafer are shown in figures 2 and 3.

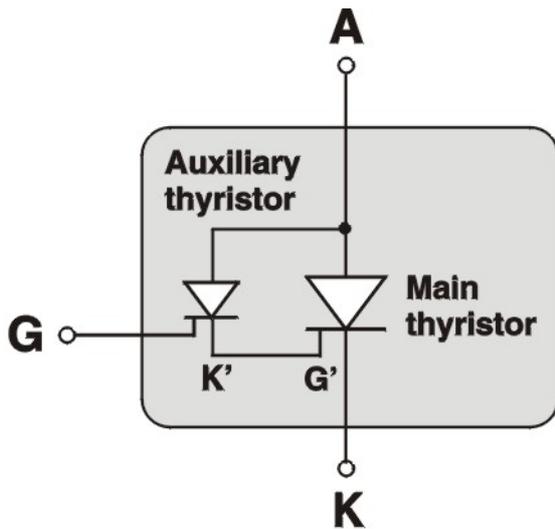


Figure 2 Basic principle of the amplifying gate.

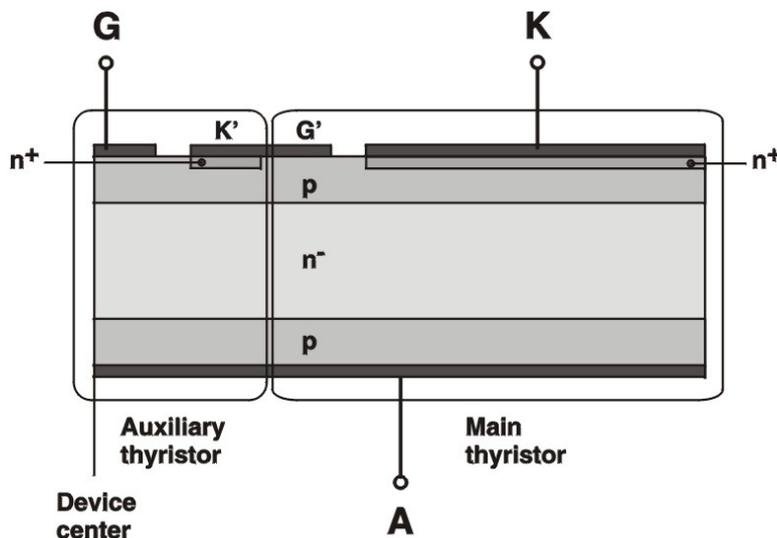


Figure 3 Lateral integration of the amplifying gate.

To further improve the turn-on behaviour of the device the auxiliary thyristor structure may be distributed over the whole thyristor area, thus accelerating the spread of the conducting regions during turn-on. This reduces turn-on losses and allows higher di/dt ratings as compared to simple central gate structures. ABB frequently use the T-gate design for the distributed auxiliary thyristor structure shown in figure 4.

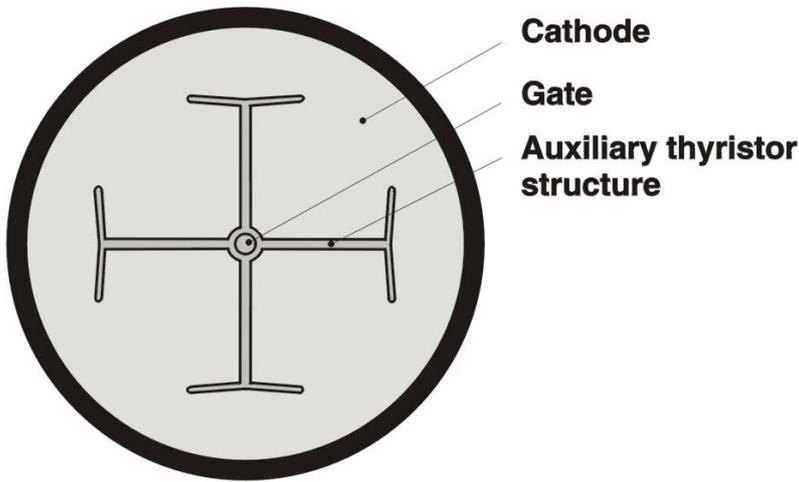


Figure 4 View of thyristor wafer with distributed gate(T-Gate).

The gate characteristics for a device with amplifying gate can be seen in figure 5. A repetitive AC gate current with peak value 10 A is applied and in figure 5, two “kinks” can easily be seen representing the triggering of the auxiliary and subsequently the main thyristor.

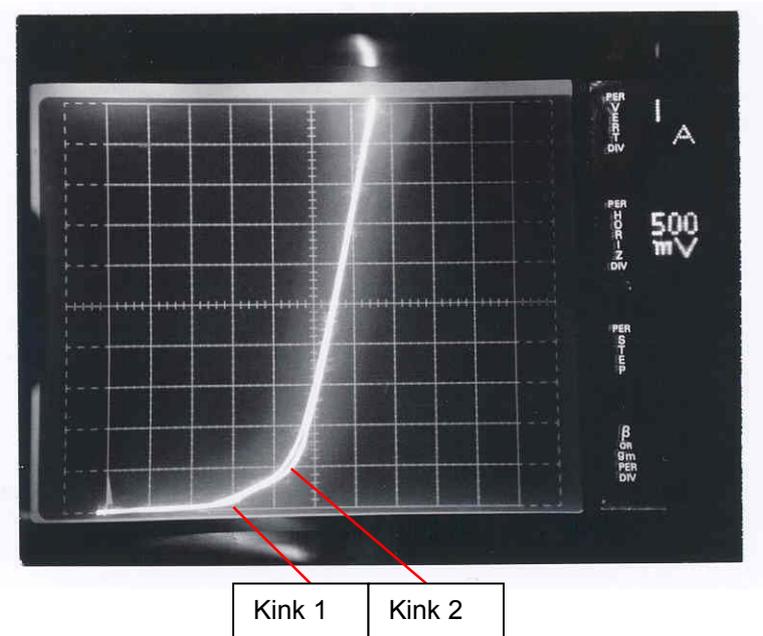


Figure 5 Amplifying gate characteristic of thyristor 5STP 26N6500.

2.3 Recommendations about gate current and gate-drive load-line

Even though a thyristor can be triggered at static conditions by a current level of I_{GT} a gate current with an amplitude of several times I_{GT} is needed for proper triggering giving the wished dynamic performance at dynamic conditions. Based on the experience that ABB has gathered during many years we recommend a gate pulse as shown in figure 6.

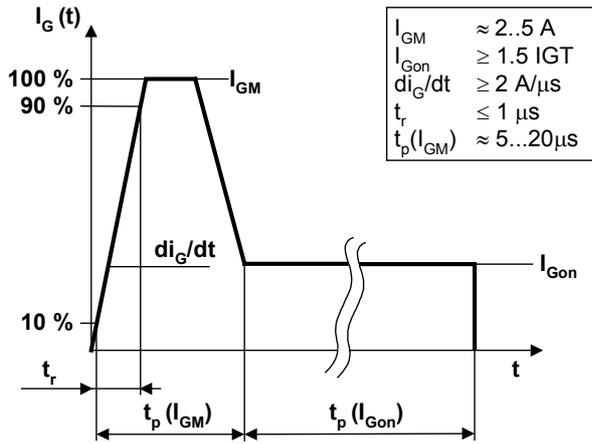


Figure 6 Recommended gate pulse for ABB phase control thyristors.

The initial part of the gate pulse, characterised by the parameters I_{GM} , di_G/dt , t_r and $t_p(I_{GM})$, strongly affects the following thyristor characteristics and ratings:

- Turn-on delay time
- Turn-on fall time of the anode voltage
- Turn-on switching energy loss
- Critical di/dt of the anode current at turn-on.

A high I_{GM} and a low t_r , i.e. a high di_G/dt enhance all of these ratings and characteristics. The importance of these parameters in various applications is discussed in the following paragraphs.

Although I_{GM} should not exceed 10 Amperes, as indicated in the data sheet (I_{FGM} rating), there is no upper device limit for di_G/dt , i.e. the gate current rise rate is only limited by the driving voltage, gate lead inductance and gate voltage. The duration of the gate current overshoot, $t_p(I_{GM})$, should be in the range specified above; 5 μs are sufficient for $di/dt \geq 20 \text{ A}/\mu\text{s}$, and 20 μs would typically be required for $di/dt \leq 5 \text{ A}/\mu\text{s}$. For very low Anode di/dt the fall time for I_{GM} should not be too short, since the device may turn off if the gate current drops too fast.

To achieve the recommended gate pulse and to avoid severe distortion of the gate current described in paragraph 2.8, the Gate-driver should be designed with a appropriate load-line. By drawing the load lines onto the gate characteristic graph the resulting gate current can be determined. Some examples are included in figure 7.

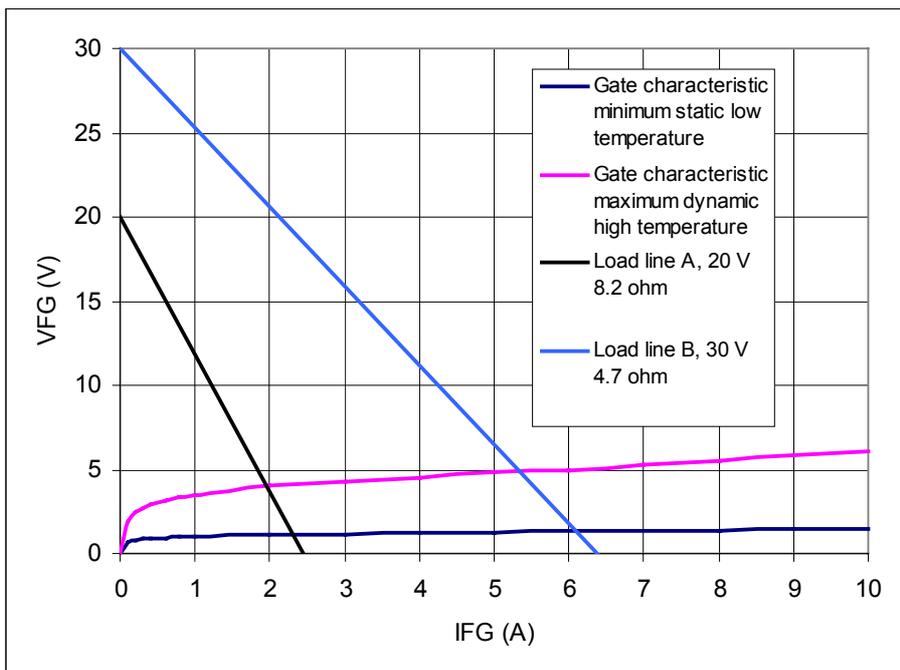


Figure 7 Gate-driver load line examples.

Load line A, 20 V 8.2 Ω , resulting in a gate current of about 2 A at dynamic conditions, shows a load line that can be considered as an acceptable design for normal applications and load line B, 30 V 4.7 Ω , resulting in a gate current of about 5.5 A at dynamic conditions, is an example what can be recommended for high di/dt applications and for applications with series- and parallel-connected thyristors.

2.4 Recommendations for Crow-bar and other high di/dt applications

That the conduction area of the thyristor is initially quite small is for many line-commutated applications not a major issue since the rate-of-rise of load current is moderate and matched by the rate-of-rise of conducting area. For other applications however with either a high repetitive rate-of-rise of load current or with single pulses with high di/dt and high peak current, the relatively slow rate of increase of conducting area represent a potential danger due to the high current density close to the gate region. Since this region has poorer cooling due to the gate contact, there is a risk for local over heating leading to device failure. A strong initial gate pulse will ensure that the amplifying gate and the main gate fire homogeneously allowing maximal device ratings to be achieved. A weak gate pulse may lead to localised gate current and consequent local anode current flow resulting in a hot-spot with subsequent device failure. It should be mentioned that pressure homogeneity is essential for a full di/dt capability. Pressure homogeneity can be verified using Fuji pressure film, details at www.fujiprescale.net, or similar products from other vendors

Another risk at very high di/dt is the dynamic potential difference between gate and cathode. This voltage comes from the lateral gate current flow in the finger structure and can lead to flash overs between gate and cathode and is a further limitation to the non-repetitive di/dt performance. The di/dt performance can be increased somewhat by the use of a Gate-driver with a sufficiently high driving voltage.

For high di/dt applications such those as "Crow bars" di/dt can be initially limited by the use of a saturable inductor. This allows the thyristor to expand the conduction area around the gate before the inductor saturates and the high di/dt occurs.

2.5 RC-snubber and parasitic capacitance discharge

Very high di/dt in many thyristor applications comes from snubber dump, discharge of parasitic cable capacitances and parallel capacitances. The latter are sometimes used in systems with series connected thyristors which ensure that all thyristors get an initial high current peak to get the devices turned-on simultaneously. In some cases current peaks comes from voltage dividing capacitors used for voltage sharing with the transformer capacitance. This to reduce the voltage stress on the converter in case of fast surges on the supply line. In all these cases the current rises very steep, sometimes several 100 A/ μ s or even above 1000 A/ μ s, when the thyristor triggers since the loop resistances and inductances are quite small. Depending on device design, the maximum current peak allowed for current pulses with very high di/dt is 100 – 300 A with some devices able to handle 400 A. This rating is not specified in the ABB thyristor data sheets but is indirectly included since the rated di/dt is measured with an application typical RC-circuit. The data sheet rating is though for the main current rate-of-rise only. The peak current from the discharge of this RC-circuit is normally in the range of 50 – 100 A and to this a small current from the stray capacitance in the measurement system is added. The influence of additional capacitance has for some devices been tested by parallel connection of discrete capacitors to simulate the stray capacitance. One example from a test is seen in figure 8. A gate pulse as recommended in figure 6 is in most cases suitable to handle these currents.

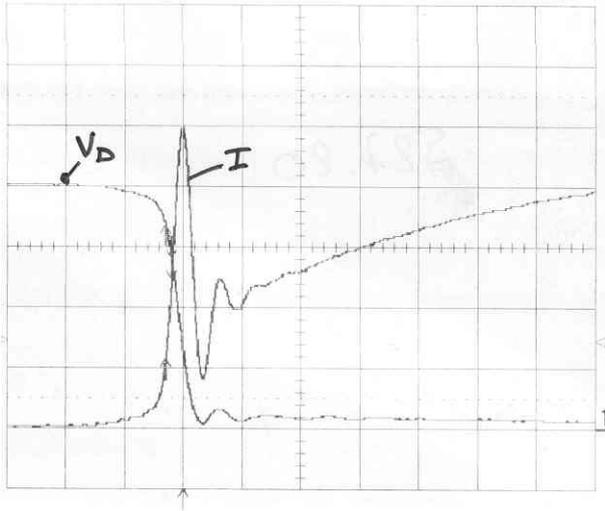


Figure 8 Discharge of 20 nF parasitic capacitance using 5STP 25L5200 at $V_d = 4000$ V, $t = 0.5 \mu\text{s}/\text{div}$, $I = 100$ A/div, $T_j = 90$ °C.

2.6 Back-porch currents and picket fence current pulses

"Back-porch current" (I_{Gon}) is required to keep the thyristor in the on-state when the anode current falls below the holding current I_H , typically in discontinuous current mode in controlled rectifiers, or line voltage reverses. Ideally a thyristor is fired when forward biased but the Gate-driver signal cannot always be synchronised with the load current. Back-porch current ensures that the thyristor will start conduct or conduct once more when the anode voltage becomes positive again. It is recommended to use a back-porch current, $I_{Gon} \geq 1.5 \cdot I_{GT}$ where I_{GT} is the minimum gate trigger current at the minimum junction (or ambient) temperature.

As stated in next paragraph care should though be taken to minimise the time when gate current is given to the device when it is reverse blocking, may it be through synchronisation problems or to long back-porch current pulse length.

To reduce the power needed for the gate unit I_{Gon} is often realised with "picket fence" current pulses as illustrated in figure 9.

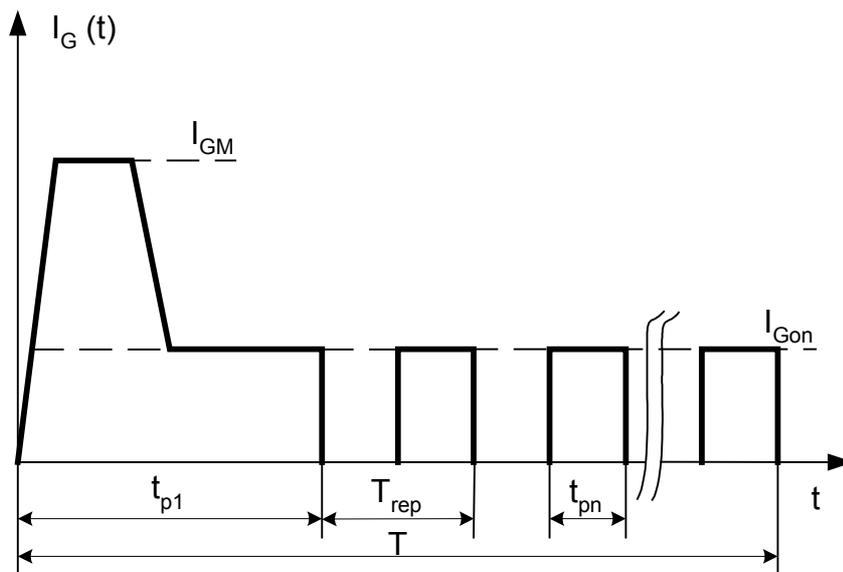


Figure 9 Example of a picket fence gate pulse.

The duration of the back porch current must be long enough to ensure that the thyristor is able to trigger at any time in the prospective conduction period, see discussion above (I_{Gon}). It is recommended to have the first pulse t_{p1} longer than $30 \mu\text{s}$ and to have a duty cycle $t_{pn}/T_{rep} \geq 0.5$. Typical values for T_{rep} are $20 - 100 \mu\text{s}$.

2.7 Gate current during reverse blocking

When the thyristor is in its reverse blocking state, there is no risk of triggering by a positive or negative gate current. However, applying reverse anode voltage and positive gate current simultaneously will lead to an increased leakage current. A reverse biased thyristor will act as a transistor with a gain in the range of 0.1 – 0.5. A gate current of 1 A can increase the leakage current with some 100 mA even at room temperature. This leakage current can at certain circumstances lead to devices failure and should be avoided, even though it in special cases cannot be avoided. An example of the transistor action is seen in figure 10.

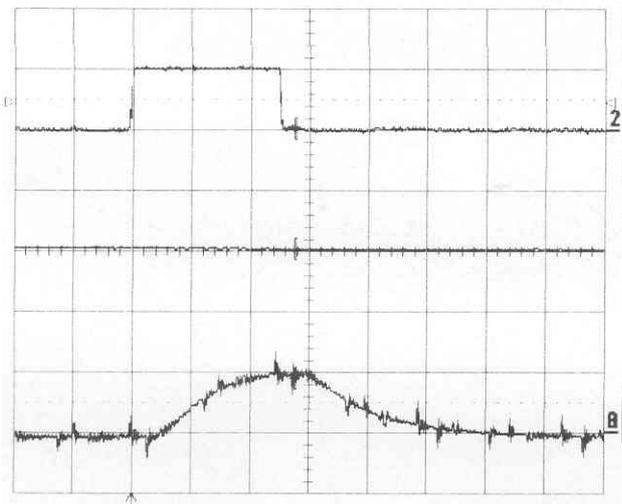


Figure 10 Leakage current increase due to gate current for 5STP 25L5200 at $V_R = 1500$ V, $I_G = 2$ A(channel 2), $T_j = 100$ °C, $I_r = 200$ mA/div(channel B), $t = 20$ μ s/div.

2.8 Gate current distortion

At the beginning of this application note, it was stated that the gate voltage is the reaction of the thyristor to the applied gate current. In the first phase of the turn-on process, the gate-to-cathode impedance is higher than the steady-state value given in the datasheet (V_{FG} vs. I_{FG}). The dynamic gate voltage is a function of the charge carrier concentration in the gate region, the internal inductances and the di/dt of the anode current. At high di/dt the amplifying gate needs a high current to turn on the main thyristor. This current is provided by the auxiliary thyristor and it lifts the gate voltage due to the impedance of the distributed gate structure.

With the recommended gate pulse, the peak gate voltage V_{GM} can reach amplitudes of 12 Volts or more. This has to be considered when the supply voltage source for the gate pulse amplifier and the gate pulse transformer are designed. If the open circuit Gate-drive voltage is too low, the gate current may be considerably distorted, $I_G(t)$ can have an instantaneous minimum close to zero or even have a severe distortion where $I_G(t)$ briefly becomes negative. Both cases can be dangerous for the thyristor and may lead to failure. This behaviour also needs to be considered when designing the thyristor Gate-driver since it must be able to withstand a negative gate current without destruction. This is often accomplished by the use of a Diode, preferably a Schottky-Diode, in series with the Gate-driver as shown in figure 11.

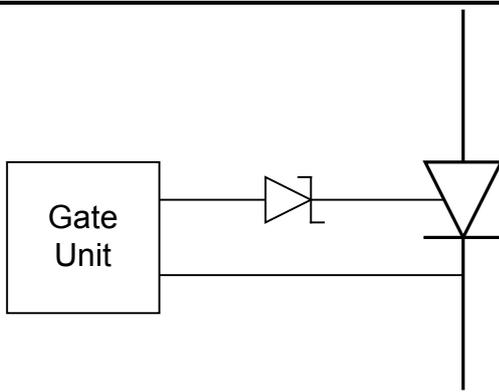


Figure 11 Simplified circuit drawing showing the incorporation of a Schottky-Diode to protect the Gate-drive.

In this context it is recommended that the design of the gate unit allows for gate current measurements under worst-case conditions (max. anode di/dt), where possible. A Gate-drive supply voltage of ≥ 20 V for moderate di/dt applications and ≥ 30 V for high di/dt requirements is recommended. One example of a very strong gate current distortion when the Gate-driver voltage is lower than the dynamic gate voltage of the device is shown in figure 12.

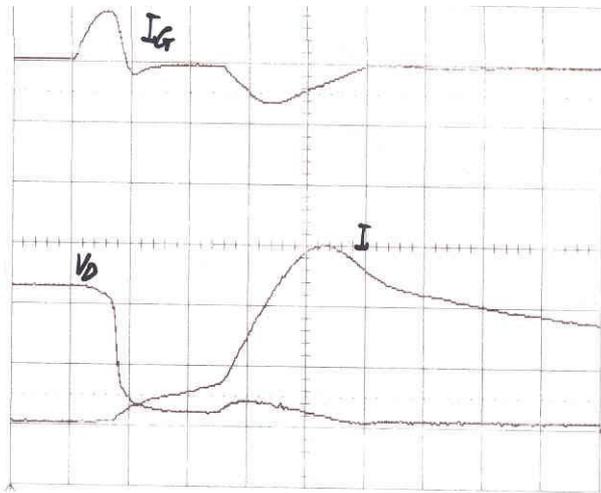


Figure 12 Gate current distortion at very high di/dt, $t = 2 \mu\text{s}/\text{div}$, $I_G = 5 \text{ A}/\text{div}$, $V_D = 2\text{kV}/\text{div}$, $I = 1 \text{ kA}/\text{div}$, thyristor 5STP 12N8500 at $T_j = 90^\circ\text{C}$.

2.9 Triggering considerations at serial and parallel connection of thyristors

Series Connected Thyristors:

At turn-on it is important that all individual devices switch simultaneously, otherwise the slower devices may be subjected to over-voltage. Beside the importance of simultaneous trigger signals for all devices, differences in delay times, Δt_d , in a stack of series connected PCT's, must be minimised by the application of a strong gate pulse which limits the absolute value of t_d itself. Voltage imbalances at turn-on, which will always be present because of parametric scatter and different junction temperatures, are the further reduced by the RC snubber circuit across the device. The RC snubber is needed in most applications anyway to limit voltage overshoot during reverse recovery

Parallel Connected Thyristors:

The imbalance in the turn-on characteristics of parallel connected thyristors is also minimised by a strong gate pulse applied simultaneously to all devices. This is important for good current sharing during the dynamic turn-on phase. Normally there is no need to select devices regarding t_d to get a good current sharing but in rare cases it may be needed.

2.10 Spurious triggering due to Electro-magnetic interference

Thyristors are operated in electrically noisy environments. In order to minimise the inductance of the gate lead, and through that the noise sensitivity, it is advantageous to mount the Gate-driver as close as possible to the thyristor and to twist the gate leads or to use coaxial cables. Care must be taken that gate leads are not in contact with high voltage or high current parts in order to avoid electromagnetic interference or even flash-over to the gate leads. Sometimes a gate filter may be needed but then cautions must be taken so the device still gets a proper gate pulse since the filter will tend to reduce it.

To determine what interference levels of short duration that can trigger devices, tests has been done on device 5STP 28L4200 at the following conditions:

For gate pulses with duration about 1.5 μ s and with $V_D = 200$ V the current levels needed to trigger the thyristors were:

At $T_c = 25$ °C, $I_G = 495 - 655$ mA with average value 590 mA.

At $T_c = 50$ °C, $I_G = 460 - 560$ mA with average value 517 mA.

At $T_c = 80$ °C, $I_G = 390 - 530$ mA with average value 472 mA.

3 Additional notes

3.1 Trigger signal transmission to and power supply for the Gate-drive unit

Since the thyristors are at line potential and the control system in most cases are low voltage circuits at ground potential, the gate signal to the thyristor must be galvanically separated from the control system. There are several possibilities to accomplish this and the design is normally done depending on the voltage level in the system. For low voltage systems the gate current is transferred through a pulse transformer that provides the required insulation. For medium and high voltage systems the gate pulse is often generated on a PCB at high potential. The common design is to send the gate pulse from the control unit through an optical fibre to the Gate-driver which gets its power either from an insulated power supply or from the anode voltage. Another design is to send a high energy pulse through a closed loop that through induction is transferred to the Gate-drive giving both timing and energy for the gate pulse to the thyristor. This design is less prone to spurious triggering since the Gate-drive is only energised when the pulse current is active.

It is important to design the Gate-driver so that the main circuit does not influence the gate pulses via capacitive or inductive coupling caused by the presence of high dv/dt and di/dt . This is particularly important when several functionally independent thyristors are fired by the same driver board.

3.2 Application support

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